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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/749,660	12/28/2000	Manoj Kharc	2207/9865	8718

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KENYON & KENYON LLP  
1500 K STREET N.W.  
SUITE 700  
WASHINGTON, DC 20005

EXAMINER
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THAI, TUAN V

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/749,660

**Applicant(s)**

KHARE ET AL.

**Examiner**

Tuan V. Thai

**Art Unit**

2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE \_\_\_\_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on RCE (7/5/5) and communication (7/14/5).
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) 7 and 28 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6, 8-27 and 29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 April 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |                                                                                                                         |                                                                                         |
|-------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                             | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date: ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date: ____. | 6) <input type="checkbox"/> Other: ____.                                                |

**Part III DETAILED ACTION**

***Specification***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 05, 2005 has been entered.
2. Claims 1-6, 8-27 and 29 are presented for examination. Claims 7 and 28 have been cancelled.
3. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.
4. The objection to claim 2 is hereby withdrawn due to amendment filed July 05, 2005.

***Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section

102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-6, 8-27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baumgartner et al. (USPN: 6,275,907); hereinafter Baumgartner; in view of Arimilli et al. (USPN:5,895,484); hereinafter Arimilli.

As per claim 1, Baumgartner discloses the invention as claimed including a method for reducing memory latency in a multi-node architecture [6] comprises issuing a memory request from a requesting node (e.g. see column 9, lines 12 et seq., figure 3A); issuing a speculative memory request from a coherent agent in response to the memory read request from the requesting node (e.g. see column 9, lines 25 et seq.; for example, the speculative memory read request must be issued by the remote processing node 8 in order for the TSU 42 to determine if coherence directory 50 indicates that the requested cache line is checked out to a remote processing node 8 in modified state); receiving the speculative memory read request at a home node before results of a cache coherence protocol (MESI) are determined (e.g. see column 4, lines 29 et seq.; lines 63-67; figure 3A, block 90; and column 9, lines 18 et seq.); initiating a read to memory to complete the speculative memory read request (e.g. see column 9, lines 34 et seq.). Baumgartner, with one

exception, does not particularly teach completing said memory read request before results of the cache coherence protocol are determined. Arimilli, in his teaching of method and system for speculatively accessing a cache memory data within a multiprocessor data-processing system; clearly discloses the missing element that known to be required in the system of Baumngartner in order to arrive at Applicant's current invention wherein Arimilli discloses completing speculative memory read request prior to the determining/ receiving of the cache coherence protocol (e.g. see column 5, lines 66 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to employ the teaching of Arimilli by allowing the completing of the memory read request before results of the combined cache coherence protocol are determined for that of Baumngartner's invention. By doing so, Arimilli clearly states that it would tremendously reduce the intervention latency and the overall SMP system performance is significantly improved, therefore being advantageous (e.g. see column 6, lines 1-3).

As per claim 2, buffering results of the read to memory is equivalent taught as once the requested cache line is supplied to cache hierarchy of the processor, the requested cache line is loaded into a register/buffer within processor core 12 (e.g. see column 9, lines 40-43);

As per claims 3 and 4, dropping the results of the read to

memory on a buffer full condition or if a cancel command is received is equivalently taught as canceling a load-reserve instruction if cancel command is received, then reissue the read to complete memory request; also noted the Rerun of the read request and retry of the AStaIn vote (e.g. see column 8, lines 21 et seq.; column 9, lines 52 et seq.; column 10, lines 7-8, also lines 61 et seq.);

As per claim 5, Baumgartner discloses forwarding results of the second read to memory requester (e.g. column 12, lines 54 et seq.);

As per claim 6, Baumgartner further discloses that if a confirm command is received before results of the speculative memory read which issued by the requesting node are dropped, forwarding the results of the read to a requester as being equivalent to if a determination is made at block 192 that a reservation cancelling event has not been detected, the process proceeds directly to block 200 (e.g. see column 13, lines 8 et seq.);

As per claim 8, Baumgartner discloses receiving the results of the read at the coherence agent and forwarding the results of the read to the requesting node memory (e.g. see column 10, lines 35-38);

As per claim 9, Baumngartner discloses the invention as claimed including a method for reducing memory latency in a multi-node architecture [6] comprises issuing a memory request by

a requesting node (e.g. see column 9, lines 12 et seq., figure 3A); issuing a speculative memory request from a coherent agent to a home node in response to the memory read request from the requesting node (e.g. see column 9, lines 25 et seq.; for example, the speculative memory read request must be issued by the remote processing node 8 in order for the TSU 42 to determine if coherence directory 50 indicates that the requested cache line is checked out to a remote processing node 8 in modified state; also see column 4, lines 29 et seq.; lines 63-67; figure 3A, block 90; and column 9, lines 18 et seq.); initiating a read to memory that the home node is taught as data stored within each system memory 18 **can be requested, accessed,** and modified by any processor 10 within NUMA computer system 6 (e.g. see column 5, lines 3 et seq.); initiating the cache coherency protocol (e.g. see column 7, lines 16 et seq.). Baumgartner, with one exception, does not particularly teach completing said memory read request before results of the cache coherence protocol are determined. Arimilli, in his teaching of method and system for speculatively accessing a cache memory data within a multiprocessor data-processing system; clearly discloses the missing element that known to be required in the system of Baumgartner in order to arrive at Applicant's current invention wherein Arimilli discloses completing speculative memory read request prior to the determining/receiving of the cache coherence protocol (e.g. see column 5, lines 66 et seq.). Accordingly, it

would have been obvious to one having ordinary skill in the art at the time the current invention was made to employ the teaching of Arimilli by allowing the completing of the memory read request before results of the combined cache coherence protocol are determined for that of Baumgartner's invention. By doing so, Arimilli clearly states that it would tremendously reduce the intervention latency and the overall SMP system performance is significantly improved, therefore being advantageous (e.g. see column 6, lines 1-3).

As per claim 10; updating a memory status relating to the results in a table after the results of the cache coherence protocol (e.g. see column 5, lines 59 et seq.);

As per claim 11; initiating a status look-up to determine the caching status of the requested memory (e.g. see column 7, lines 21 et seq.);

As per claim 12, Baumgartner discloses issuing a command to the home node if the caching status is determined to be in an invalid state or shared state (e.g. see column 4, lines 29 et seq.);

As per claim 13, snooping a node with the exclusive copy of the requested memory cache (e.g. see column 8, lines 33 et seq.; column 11, lines 30 et seq.);

As per claims 14 and 15, determining whether the exclusive copy of the requested memory is clean or dirty, and issuing a confirm command for clean requested memory (e.g. see column 11,



lines 33 et seq.; also see table VI);

As per claim 16, the further limitation of issuing a cancel command to the home node if the exclusive copy of the requested memory is dirty (being modified) is embedded in the system of Baumgartner and being taught to the extent that it is being claimed, for example, Baumgartner clearly discloses the cache line which is remotely held can make a transition from Exclusive to Modified (dirty), in addition with the implementation of the MESI protocol, the cancellation of the requested command should be existed in order to guarantee the coherency within the system;

As per claim 17, Baumgartner discloses receiving a snoop result which includes a copy of the requested memory and updating a memory status relating to the requested memory in a table (e.g. column 7, lines 21 et seq.; table VI);

As per claim 18, Baumgartner discloses receiving the requested memory and forwarding the requested memory to a requesting node (e.g. see column 10, lines 35-38);

As per claims 19-27 and 29, they encompass the same scope of invention as to that of claims 1-6, 8 and 9-18 except they are drafted as apparatus format rather than method format, the claims are therefore rejected for the same reason as being set forth above; noting that Baumgartner discloses processor 12, system memory 18 and node controller 20 as being illustrated in figure 1, column 3, lines 10 et seq.);

7. As per remark, Examiner would like to emphasize that the issuing of a speculative memory request from a coherent agent in response to the memory read request from the requesting node is taught by Baumgartner; for example, the speculative memory read request must be issued by the remote processing node 8 in order for the TSU 42 to determine if coherence directory 50 indicates that the requested cache line is checked out to a remote processing node 8 in modified state (e.g. see column 9, lines 25 et seq.;). In considering a 35 USC 103 rejection, it is not strictly necessary that a reference or references explicitly suggest the claimed invention (this is tantamount to a 35 USC 102 reference if the modifications would have been obvious to those of ordinary skill in the art. It has been held that the test of obviousness is not whether the features of a secondary reference may be bodily incorporated into the primary references' structure, nor whether the claimed invention is expressly suggested in any one or all of the references; rather, the test is what the combined teachings of the reference would have suggested to those of ordinary skill in the art. See In re Keller et al., 208 U.S.P.Q 871. In addition, Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975).

However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). Baumgartner and Arimilli references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969. In this case, the Arimilli reference was used to provide evidence of completing of the read memory request by a coherency agent before results of the cache coherence protocol are determined; for example, Arimilli discloses that by allowing the requested data to be read from the L2 cache of the intervening processing unit before the combined coherency response is received, the intervention latency is reduced tremendously and the overall SMP system performance is significantly improved (e.g. see column 5, line 66 bridging column 6, line 3). Therefore, the 103 rejection based on incorporating the well known of bit by bit level comparison, as evidenced by Arimilli, into Baumgartner's system is deemed to be proper.

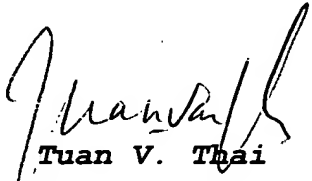
#### **Conclusion**

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
9. Any inquiry concerning this communication or earlier

communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**TVT**/August 04, 2006

  
Tuan V. Thai  
**PRIMARY EXAMINER**  
Group 2100